UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,747	04/23/2001	Howard Sachs	021111000100	4810

20350 7590 03/28/2003

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER
BOWERS, BRANDON

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,747	SACHS, HOWARD	
	Examiner	Art Unit	
	Brandon W Bowers	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-32* is/are pending in the application.

4a) Of the above claim(s) *1-10 and 27-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11 and 13-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II – Claims 11-26 in Paper No. 5 is acknowledged. Cancellation of claims 1-10 and 27-32 is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andreev, US Patent No. 6,182,272 in view of Josephson et al., US Patent No. 6,532,580.

In reference to claim 11, Andreev teaches a method comprising obtaining cells, laying out cells and trace routing (Figure 3). Andreev describes cells as being a group of one or more circuit elements grouped to perform a function. The step of obtaining cells is equivalent to selecting an item, the item being a group or a function, for placement on a layout and selecting a further item for placement on a layout. The step of laying out cells is equivalent to placing the 1st and 2nd items on the layout. The step of trace routing is equivalent to defining interconnections between the 1st and 2nd items. Andreev does not teach wherein all intra-group interconnections are defined as residing on fewer than all of the plurality of layers, and all the inter-group inter-connections

between the 1st and 2nd items reside entirely on layers not used for intra-group inter-connections. Josephson teaches a layout methodology wherein the lowest layers are used exclusively for intra-group inter-connections and the higher-level layers are used exclusively for inter-group inter-connections(column 4, lines 13-18). Accordingly, it would have been obvious at the time of invention to select and place a first and second item in a layout as taught by Andreev wherein the intra-group connections are defined as residing on fewer than all the layers, and defining inter-group inter-connections on layers not used for intra-group inter-connections as taught by Josephson to make a method comprising: when the intra-group inter-connections are defined, providing all such inter-connections on fewer than al of the plurality of layers; selecting an item, the item being a group or function for placement on a layout; placing the item on the layout; selecting a further item; placing the further item on the layout; and defining inter-group inter-connections between the item and the further item such that the inter-group inter-connections reside entirely on layers not used for the intra-group inter-connections because separating the intra-block and inter-block inter-connections onto different layers helps to eliminate the rip-up and re-route process.

In reference to claims 13, Andreev teaches wherein the plurality of layers are each layers having electrically conductive material thereon, with vias from at least one adjoining layer connected thereto (Figure 1, and Column 1, lines 42-49).

In reference to claims 13, Josephson teaches wherein the plurality of layers are each layers having electrically conductive material thereon, with vias from at least one adjoining layer connected thereto (Figure 2).

Claims 14 to 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhen, US Patent No. 6,298,468 in view of Dangelo et al, US Patent No 5,880,971, in view of Josephson et al., US Patent No. 6,532,580.

In reference to claim 14, Zhen teaches an integrated circuit comprised of a plurality of regularly placed circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups (Figure 2). Zhen does not teach that the circuit groups are on the order of1000 gates. Dangelo teaches that design methodology wherein circuit groups are less than a few thousand gates (column 13, line 42). "on the order of a 1000 thousand gates" and a few thousand gates are deemed to be equivalent to one another. It would be obvious at the time of invention to incorporate the methodology of Dangelo wherein circuit groups are less than a few thousand gates with the integrated circuit of Zhen comprised of a plurality of regularly placed circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups to make an integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups because the seemingly insurmountable job of designing a highly complex circuit is broken into small, workable design projects on an order on magnitude of 1000 gates. Zhen in view of Dangelo does not teach that each group has interconnections within that group on a plurality of layers of the integrated circuit the plurality of layers being less than all layers. Josephson teaches a layout methodology wherein the lowest layers are used exclusively for intra-

group inter-connections and the higher-level layers are used exclusively for inter-group inter-connections(column 4, lines 13-18). Accordingly, it would have been obvious at the time of invention to incorporate the methodology of Dangelo wherein circuit groups are less than a few thousand gates with the integrated circuit of Zhen comprised of a plurality of regularly placed circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups to make an integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups and further incorporate the teachings of Josephson wherein the lowest layers are used exclusively for intra-group inter-connections and the higher-level layers are used exclusively for inter-group inter-connections to make a integrated comprising a plurality of regularly placed groups, the circuit groups being on the order of 1000 gates, the circuit groups having predefined connection points , each group having interconnections within that group on a plurality of layers of the integrated circuit, the plurality of layers being less than all of the layers, at least some of the circuit groups being amalgamated into sets of groups because separating the intra-block and inter-block inter-connections onto different layers helps to eliminate the rip-up and re-route process.

In reference to claims 15-18, Zhen teaches that glue logic is used to connect the groups together (column 5, lines 35-36). Glue logic refers to the electronic circuitry required to interface two or more circuit blocks. When circuit blocks are assembled into

a larger circuit, it is common to put electronic circuitry (or electrical connections) between the circuit blocks to couple and make them operate together. The circuitry that sits between circuit blocks is called glue logic. Glue logic is equivalent to trailers and provides physical translation, buffering, and staging of interface signals associated with the predefined connection points of circuit blocks.

Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhen, US Patent No. 6,298,468 in view of Dangelo et al, US Patent No 5,880,971 in view of Josephson et al., US Patent No. 6,532,580.as applied to claim 14 above, and further in view of Block et al., Us Patent No 6,397,375.

In reference to claim 19, Zhen in view of Dangelo in view of Josephson does not teach wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers. Block teaches a plurality of metal layers wherein circuit groups and intra-block routing is on the lowest levels, while inter-block routing is on the higher level. Additionally clock and power signals are on all layers (Column 2, lines 4-11). Accordingly, Block teaches wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers. Accordingly it would be obvious at the time of invention to integrate the circuit as taught by Block wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals

on metal layers other than the first plurality of metal layers with the integrated circuit of Zhen, Josephson, and Dangelo as described above in claim 14 to create an integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups each group having interconnections within that group on a plurality of layers of the integrated circuit, the plurality of layers being less than all of the layers, wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers because as integrated circuits of increasingly higher densities have been developed, more metal layers and interconnects per layer are required.

In reference to claims 20-22, Block teaches wherein clock and power signals are on the same layer, wherein global routing signals are on a different layer than the first plurality of layers and the clock and power signals, and the global routing signals are on a plurality of layers (Column 2, lines 4-11).

In reference to claims 23-26, Dangelo teaches wherein the groups comprise data path groups, memory groups, control groups, I/O groups, and analog groups (Figure 1 and column 7, lines 7-54).

Response to Arguments

Applicant's arguments with respect to claims 11-18 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's arguments, the recitation groups of the order of 300-5000 gates has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W Bowers whose telephone number is (703)305-4387. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9313 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-1782.

BWB
March 17, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800